Ashling announce plans for OpenHW CORE-V Development Kit

Silicon Valley, November 2nd, 2021. Ashling announce plans for OpenHW CORE-V Development Kit

The OpenHW CORE-V (https://www.openhwgroup.org/) group are currently developing a range of open-source, RISC-V ISA based cores known as CORE-V. Ashling, as an OpenHW member, are actively involved in working on the definition and implementation of a CORE-V Development Kit which includes a reference board designed around a CORE-V MCU and an SDK containing everything needed to develop software to run on the board.

One cool feature of the CORE-V MCU is that it has on-board FPGA fabric allowing you to accelerate or turbo-charge your application by implementing some key functionality in “hardware”. We will be providing the open source Symbiflow (https://symbiflow.github.io/) tools in the SDK to support this. You could also think of this as a safe sandbox for software folk to try out some Verilog development …squeezing every possible performance cycle from the device.

Our overriding goal is to make the Kit “Plug&Play” (or to work “out-of-the-box” for those of you who remember when software was shrink-wrapped). Either, or, we want you up and running in minutes…whether it be downloading and running a simple blinky example or building a CORE-V ‘C’ Edge AI application utilising an on-board FPGA based neural network accelerator.

About Ashling

Ashling have been a leading provider of Embedded Development Tools & Services since 1982 with design centres in Limerick Ireland and Chennai India and sales and support offices in Europe, Asia Pacific, the Middle East and America. We have over thirty years’ experience in developing tools for embedded systems engineers including Debug Probes, High-speed Trace Probes and Reference Boards supporting a broad range of MCU, SoC and Soft (FPGA) based designs. Our software tools include SDKs, IDEs, Debuggers, Compilers and Simulators and we support all the main embedded architectures including RISC-V, Arm, Synopsys ARC, MIPS, Power Architecture and DSPs through our ***RiscFree™*** platform. We have a particular focus on RISC-V and are the first company to bring tools to the market supporting heterogenous debug of RISC-V cores along with cores from other vendors (e.g. Arm Cortex cores). Visit www.ashling.com for more details.