Accelerating SoC Development: A Collaborative Approach by Tenstorrent and Ashling

December 4th, 2024 – Silicon Valley, CA – Tenstorrent and Ashling announce a major advancement in SoC development, targeting software bring up and removing debug bottlenecks to accelerate development cycles.

With the growing complexity of SoCs, Tenstorrent, in collaboration with Ashling, is tackling the significant bottleneck of SoC software and hardware bring up and debug times. Traditionally, initial software bring up has depended heavily on test chips, requiring either silicon or FPGA prototypes. Our joint approach enables parallel software bring up alongside hardware design using both Simulation and/or Emulation platforms. This shift eliminates the dependency on physical hardware, reducing both cost and time, and accelerating development cycles.

Both the Simulation and Emulation platforms leverage software-defined communication between the Ashling ***RiscFree™*** debugger and the Device Under Test (DUT) within the Simulation or Emulation environment, removing the need for traditional hardware or JTAG debuggers. ***RiscFree*** is a powerful debug tool supporting Tenstorrent RISC-V cores and provides complete visibility and debug control throughout the entire software stack, from low-level device drivers to high-level application code. By incorporating JTAG transactor IP designed by Tenstorrent, the Simulation and Emulation environments can seamlessly interface with the ***RiscFree*** software stack via TCP/IP sockets, enabling efficient data exchange and debugging between ***RiscFree*** and the DUT. This gives comprehensive debugging capabilities, including breakpoints, step and execution control, register and memory inspection, real-time trace and multi-core homogeneous and heterogenous support amongst many others making ***RiscFree*** an invaluable asset in ensuring the correctness and performance of complex software systems, helping developers efficiently debug and optimize their code at every level.

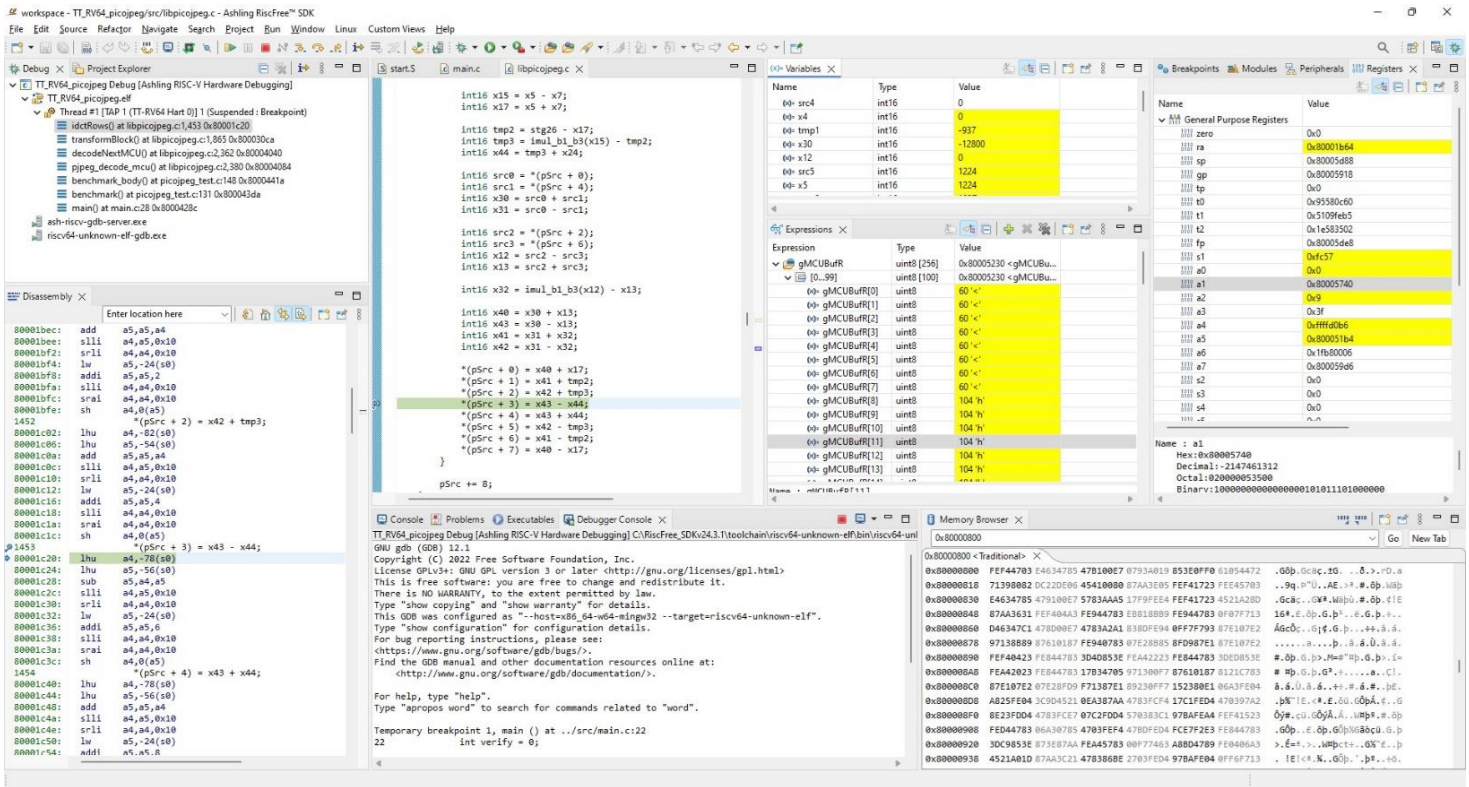

Figure 1. Ashling's *RiscFree*™ SDK Debugger debugging a Tenstorrent RISC-V core.

Not only do these approaches drive significant cost and time savings, but they also enable full emulation of the debug and trace stack in a pre-silicon environment. This provides valuable insights for evaluating and refining debug and trace and features within the design, ensuring a smoother post-silicon bring up by ensuring that software components are tested well before silicon availability, significantly reducing time-to-market and identifying integration issues earlier in the development process.

"The partnership between Tenstorrent and Ashling and leveraging of our combined expertise in RISC-V, debugging, IP design, simulation and emulation means we can bring this comprehensive solution to our customers helping them accelerate the development of complex SoC designs based on Tenstorrent's RISC-V IP. " said **Hugh O'Keeffe**, **Ashling's CEO**.

Looking ahead, Tenstorrent plans to continue to enhance the RISC-V ecosystem by contributing their ongoing work on Debug Signal Trace (DST) back to the community. RISC-V DST, first announced by Tenstorrent at the RISC-V Summit North America in October 2024, is designed to capture critical micro-architectural signals along with trace during post-silicon validation, providing invaluable data for debugging, performance analysis, and coverage directly benefiting tools like ***RiscFree*** by enabling deeper integration and more powerful features.

"By developing an open RISC-V Debug Signal Trace Specification and collaborating with the RISC-V ecosystem, we aim to enrich the capabilities available to the RISC-V community. This effort will make it easier to integrate post-silicon validation features, ensuring consistency and reducing software stack development costs. Our commitment to open-source and collaborative innovation reflects our vision of empowering the RISC-V ecosystem, driving more accessible and effective debug tools for all. We look forward to releasing these advancements and working closely with the community to accelerate the adoption of these exciting RISC-V technologies". said **Sajosh Janarthanam, Tenstorrent Lead Engineer.**

About Tenstorrent

Tenstorrent is a next-generation computing company that builds computers for AI. Tenstorrent is headquartered in North America and has locations in Toronto, Austin, and Silicon Valley, and global offices in Belgrade, Tokyo, Bangalore, Boston and Seoul, Tenstorrent brings together experts in the field of computer architecture, ASIC design, advanced systems, and neural network compilers. Tenstorrent is backed by Eclipse Ventures and Real Ventures, among others. Learn more at tenstorrent.com.

About Ashling

Ashling is a world leader in the development of tools and solutions for embedded systems and the semiconductor industry. With a focus on enabling software design for next-generation processors and SoCs, Ashling offers cutting-edge debugging tools, trace probes, and development environments. https://www.ashling.com/contact-ashling/ email:info@ashling.com.